Chip for multifunction contactless cards with function only read with 64 bit EPROM

The IZ2804-5 is intended for application in the RF identification systems. The circuit is powered by an external coil which is placed in an electromagnetic field, which is electromagnetic oscillation with the frequency 100 - 150 kHz. Master clock also received (separated) from the same field. By turning on and off the amplitude modulation current, the chip will send back the 64 bits of information contained in the memory array.

Data transfer ratio 64 periods of carrier frequency per data bit. Data is coded by the Manchester code

Application areas: access control systems in buildings, automotive guard systems, domestic animals ID systems.

Main features

- Contactless data exchange.
- Power supply from the external aerial (coil), placed in the electromagnetic field, (electromagnetic oscillations with the frequency of 125 kHz).
- Internal DC voltage limitation to prevent identifier tag fail in power electromagnetic field
- 64 bit one time programmed memory.
- data storage without power supply (non-volantive memory).
- Data transfer by means of amplitude modulation.
- Manchester coding of data.
- Temperature range from minus 45 to plus 85 ℃.
- ESD protection up to 2000 V.

Table 1 – Contact pad description

Contact pad number	Symbol	Function
01	COIL1	Coil connection I/O
02	COIL2	Coil connection I/O
03	GND	Common
04	V_{CC}	Power supply
Note – Contact pads V_{CC}, GND are purposed only for testing during IC manufacturing and are not used by customer		

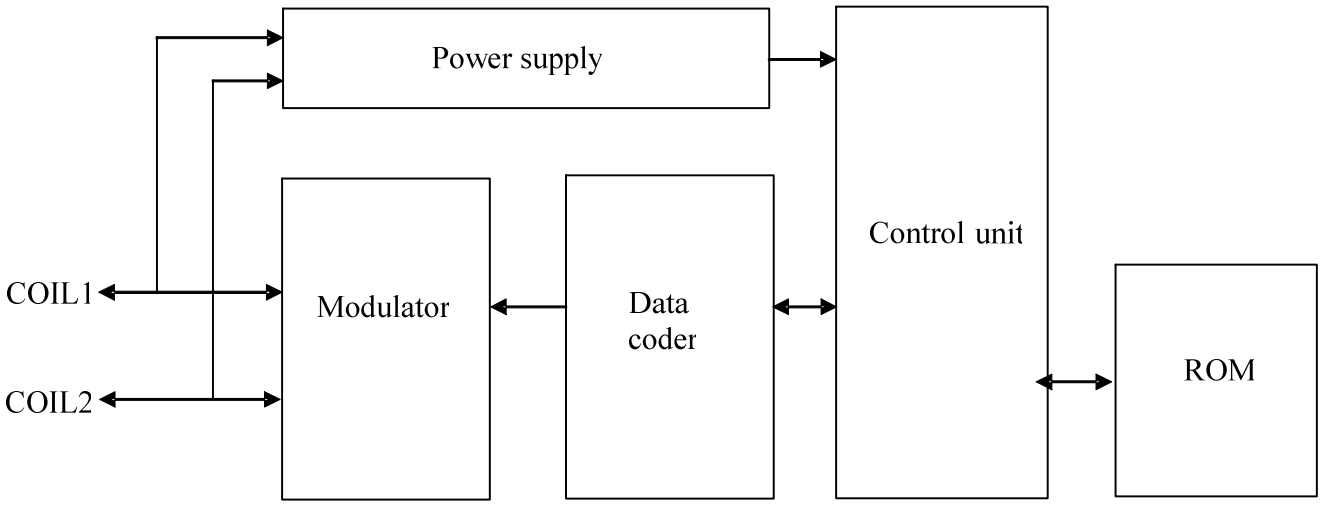


Fig. 1 – Block diagram

Table 2 Maximum ratings

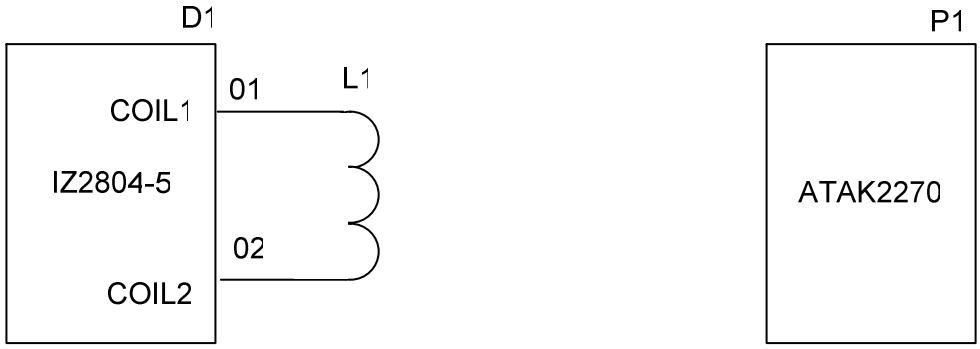
Symbol	Parameter	Target		Unit
		min	max	
U_{CC}*	Power supply voltage	- 0,3	–	V
I_I	Input current	-	30	mA
f_{COIL}	Operating frequency	-	-	kHz
T_a	Ambient temperature	- 60	125	^oC
* Internal power supply voltage rectified from external coil voltage Max supply voltage not exceed 4,5V at $I_I \leq 10$ mA (limitation is provided by design)				

Table 3 Recommended operation modes

Symbol	Parameter	Target		Unit
		min	max	
U_{CC}*	Power supply voltage	1,7	4,5	V
I_I	Input current	–	10	mA
f_{COIL}	Operating frequency	100	150	kHz
T_a	Operating ambient temperature	- 45	85	^oC
* Internal power supply voltage rectified from external coil voltage Max supply voltage not exceed 4,5V at $I_I \leq 10$ mA (limitation is provided by design)				

Table 4 – Electric parameters

Symbol	Parameter	Mode of testing	Value		Ambient temperature,^oC	Unit
			min	max		
I_{CC}	Consumption current	U_{CC}= 1,7 V	-	1,35 1,50	25±10 85 -45	uA
Imod	Current of modulator	U_{CC} = 2,8 V	0,7 0,6	-		mA
C_{RES}	Resonance capacity	f_{COIL} = 125 kHz	455	495	25±10	pF
r	Reading range	f_{COIL} = 125 kHz	9,0	-		cm



D1 – integrated circuit
L1 – inductance coil 3,38 mH (C_{RES} = 480 pF)
P1 – reader ATAK2270 or 6H10D

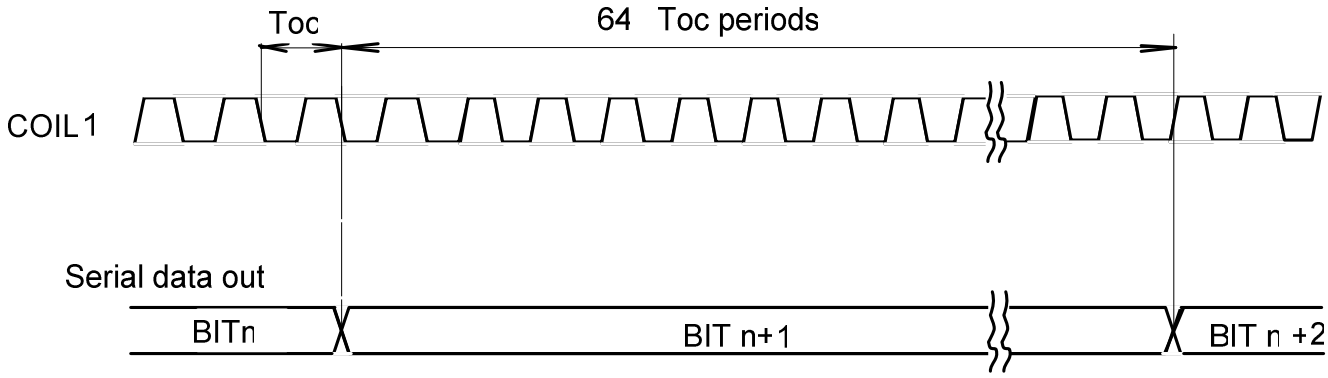
Fig. 2 – Recommended application

Operation

At chip hit in the field of the reader reading of contents of ROM, and after reading of the last of 64 bits of memory is carried out reading repeats on a cycle, since the first bit until the chip will be in the field of the reader. The continuous flow in following of data is created.

Data from the chip to a reader transferred by means of amplitude modulation of carrier frequency. Manchester coding used to represent data bits.

Read mode timing diagram is shown at Fig. 3.



Toc = $1/f_{COIL}$

Fig 3 – Read mode timing diagram

Memory structure

Structure of data memory is shown at Fig. 4.

The memory contains 64 bits divided in five groups:
- 9 bits are used for the header, ROM area (“111111111”);
- 10 row parity bits (P0-P9);
- 4 column parity bits (PC0-PC3);
- 40 data bits (D00-D93);
- 1 stop bit set to logic 0.

The header is composed of the 9 first bits which are all programmed to "1".

The header is followed by 10 data rows each consist of 4 data bits and 1 row parity bit. The last row consists of 4 column parity bits and 1 stop-bit S0 which is written to "0".

Row parity bit is set to "0" if row contain even number of bits programmed to “1”, otherwise row parity bit is set to "1”. So data array (except header) is arrange in such way that dataflow never contain more than four “1”-bits in succession. The exception - 9 bits of header programmed to "1" divides continuous dataflow to 64 bits units and serves to organize the synchronization with the reader.

Bits D_{00}-D_{03}, D_{10}-D_{13} (8 bits) define version and customer identification code. The rest of bits D_{20}-D_{93} (32 bits) – data bits, define «unique code» of chip, (see Fig. 4).

Header				00…08	(Cell number)
				“111111111”	(Cell state)
Customer code	09	10	11	12	13
	D_{00} (Cell address)	D_{01}	D_{02}	D_{03}	$P_0 = D_{00}\text{^}D_{01}\text{^}D_{02}\text{^}D_{03}$
	14	15	16	17	18
	D_{10}	D_{11}	D_{12}	D_{13}	$P_1 = D_{10}\text{^}D_{11}\text{^}D_{12}\text{^}D_{13}$
Unique code (number) of the chip	19	20	21	22	23
	D_{20}	D_{21}	D_{22}	D_{23}	$P_2 = D_{20}\text{^}D_{21}\text{^}D_{22}\text{^}D_{23}$
	24	25	26	27	28
	D_{30}	D_{31}	D_{32}	D_{33}	$P_3 = D_{30}\text{^}D_{31}\text{^}D_{32}\text{^}D_{33}$
	29	30	31	32	33
	D_{40}	D_{41}	D_{42}	D_{43}	$P_4 = D_{40}\text{^}D_{41}\text{^}D_{42}\text{^}D_{43}$
	34	35	36	37	38
	D_{50}	D_{51}	D_{52}	D_{53}	$P_5 = D_{50}\text{^}D_{51}\text{^}D_{52}\text{^}D_{53}$
	39	40	41	42	43
	D_{60}	D_{61}	D_{62}	D_{63}	$P_6 = D_{60}\text{^}D_{61}\text{^}D_{62}\text{^}D_{63}$
	44	45	46	47	48
	D_{70}	D_{71}	D_{72}	D_{73}	$P_7 = D_{70}\text{^}D_{71}\text{^}D_{72}\text{^}D_{73}$
	49	50	51	52	53
	D_{80}	D_{81}	D_{82}	D_{83}	$P_8 = D_{80}\text{^}D_{81}\text{^}D_{82}\text{^}D_{83}$
	54	55	56	57	58
	D_{90}	D_{91}	D_{92}	D_{93}	$P_9 = D_{90}\text{^}D_{91}\text{^}D_{92}\text{^}D_{93}$
	59	60	61	62	63
Column parity control	$PC_0 = D_{00}\text{^}D_{10}\text{^}D_{20}\text{^}D_{30}\text{^}D_{40}\text{^}D_{50}\text{^}D_{60}\text{^}D_{70}\text{^}D_{80}\text{^}D_{90}$	$PC_1 = D_{01}\text{^}D_{11}\text{^}D_{21}\text{^}D_{31}\text{^}D_{41}\text{^}D_{51}\text{^}D_{61}\text{^}D_{71}\text{^}D_{81}\text{^}D_{91}$	$PC_2 = D_{02}\text{^}D_{12}\text{^}D_{22}\text{^}D_{32}\text{^}D_{42}\text{^}D_{52}\text{^}D_{62}\text{^}D_{72}\text{^}D_{82}\text{^}D_{92}$	$PC_3 = D_{03}\text{^}D_{13}\text{^}D_{23}\text{^}D_{33}\text{^}D_{43}\text{^}D_{53}\text{^}D_{63}\text{^}D_{73}\text{^}D_{83}\text{^}D_{93}$	S0 = 0

Row parity control

Stop bit

Note - **^** - «XOR» logic operation

Fig 4 – Structure of data memory

Manchester code

There is always a transition from HIGH to LOW or from LOW to HIGH in the middle of bit period. At the transition from LOW to HIGH logic bit “1” is transmitted , at the transition from HIGH to LOW logic bit “0” is transmitted. (see Fig. 5).

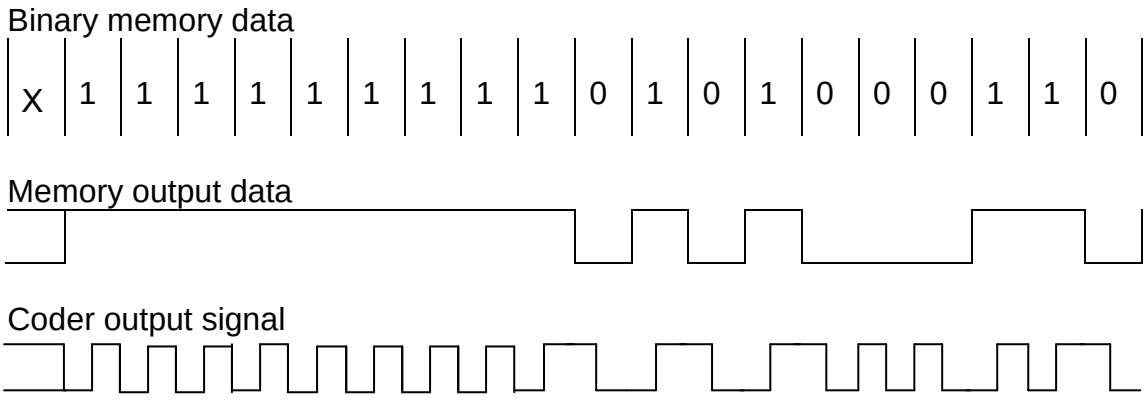
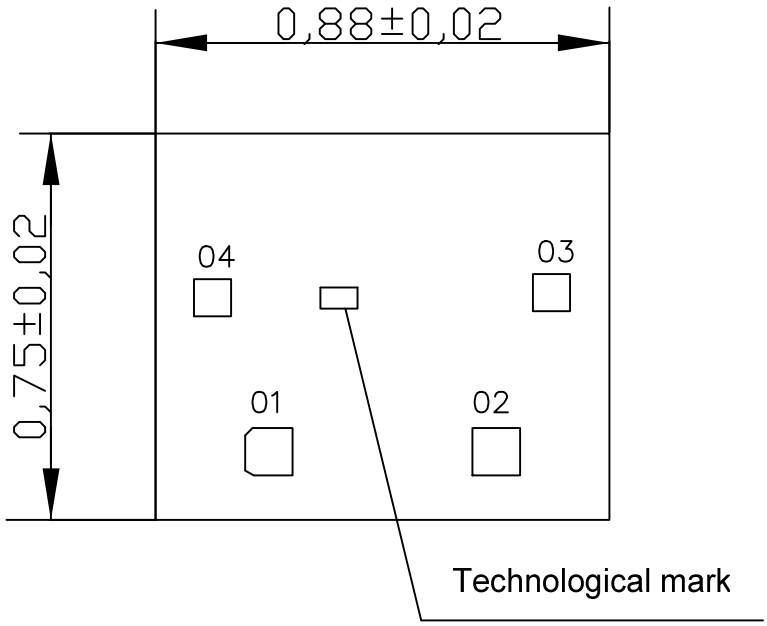


Fig. 5 Manchester code



Technological mark “IZ2804SM” coordinates (mm): left bottom corner x = 0,320, y = 0,410
Die thickness 0,18±0,01 mm.

Contact pad number	Coordinates (Left bottom corner), mm		Contact pad dimensions, mm
	X	Y	
01	0,174	0,086	0,092 x 0,092
02	0,615	0,086	0,092 x 0,092
03	0,732	0,405	0,072 x 0,072
04	0,075	0,395	0,072 x 0,072
Note: Contact pad coordinates and size are indicated under «Passivation» layer			

Fig. 6 – Chip and contact pad layout