

**IN74ACT245**

**Octal 3-State Noninverting  
Bus Transceiver  
High-Speed Silicon-Gate CMOS**

The IN74ACT245 is identical in pinout to the LS/ALS245, HC/HCT245. The IN74ACT245 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74ACT245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

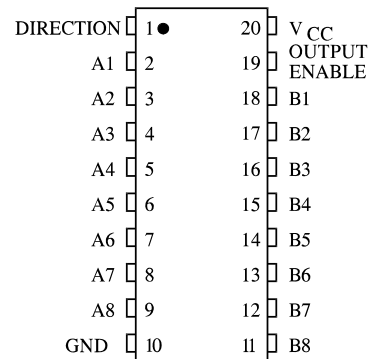
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A; 0.1  $\mu$ A @ 25°C
- Outputs Source/Sink 24 mA

N SUFFIX PLASTIC

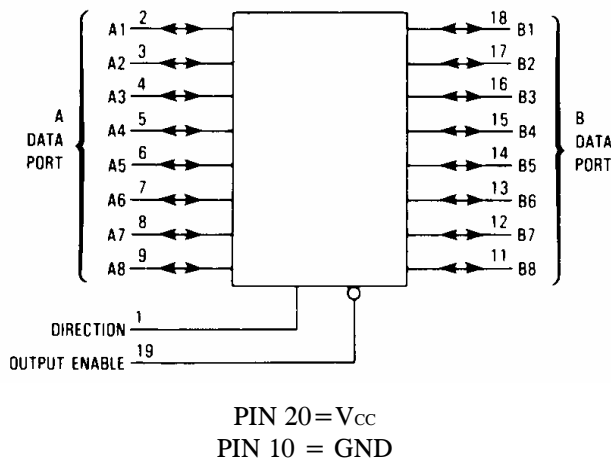
DW SUFFIX SOIC

**ORDERING INFORMATION**  
 IN74ACT245N Plastic  
 IN74ACT245DW SOIC  
 T<sub>A</sub> = -40° to 85° C for all packages

**PIN ASSIGNMENT**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

| Control Inputs |           | Operation                             |
|----------------|-----------|---------------------------------------|
| Output Enable  | Direction |                                       |
| L              | L         | Data Transmitted from Bus B to Bus A  |
| L              | H         | Data Transmitted from Bus A to Bus B  |
| H              | X         | Buses Isolated (High Impedance State) |

X = don't care

**MAXIMUM RATINGS\***

| Symbol           | Parameter  | Value                        | Unit |
|------------------|--|------------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage (Referenced to GND)  | -0.5 to +7.0                 | V    |
| V <sub>IN</sub>  | DC Input Voltage (Referenced to GND)   | -0.5 to V <sub>CC</sub> +0.5 | V    |
| V <sub>OUT</sub> | DC Output Voltage (Referenced to GND)  | -0.5 to V <sub>CC</sub> +0.5 | V    |
| I <sub>IN</sub>  | DC Input Current, per Pin  | ±20                          | mA   |
| I <sub>OUT</sub> | DC Output Sink/Source Current, per Pin   | ±50                          | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                                  | ±50                          | mA   |
| P <sub>D</sub>   | Power Dissipation in Still Air, Plastic DIP+<br>SOIC Package+                    | 750<br>500                   | mW   |
| T <sub>stg</sub> | Storage Temperature  | -65 to +150                  | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260                          | °C   |

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

| Symbol                             | Parameter   | Min  | Max             | Unit |
|------------------------------------|---|--|-----------------|------|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                 | 4.5  | 5.5             | V    |
| V <sub>IN</sub> , V <sub>OUT</sub> | DC Input Voltage, Output Voltage (Referenced to GND)  | 0  | V <sub>CC</sub> | V    |
| T <sub>J</sub>                     | Junction Temperature (PDIP)                           |  | 140             | °C   |
| T <sub>A</sub>                     | Operating Temperature, All Package Types              | -40  | +85             | °C   |
| I <sub>OH</sub>                    | Output Current - High                                 |  | -24             | mA   |
| I <sub>OL</sub>                    | Output Current - Low                                  |  | 24              | mA   |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time *<br>(except Schmitt Inputs) | V <sub>CC</sub> =4.5 V<br>V <sub>CC</sub> =5.5 V | 0<br>10<br>8.0  | ns/V |

\*V<sub>IN</sub> from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol             | Parameter                                      | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limits |               | Unit |
|--------------------|--|--|----------------------|-------------------|---------------|------|
|                    |  |  |                      | 25 °C             | -40°C to 85°C |      |
| V <sub>IH</sub>    | Minimum High-Level Input Voltage               | V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  | 4.5<br>5.5           | 2.0<br>2.0        | 2.0<br>2.0    | V    |
| V <sub>IL</sub>    | Maximum Low - Level Input Voltage              | V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  | 4.5<br>5.5           | 0.8<br>0.8        | 0.8<br>0.8    | V    |
| V <sub>OH</sub>    | Minimum High-Level Output Voltage              | I <sub>OUT</sub> ≤ -50 μA  | 4.5<br>5.5           | 4.4<br>5.4        | 4.4<br>5.4    | V    |
|                    |  | *V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OH</sub> = -24 mA<br>I <sub>OH</sub> = -24 mA                                      | 4.5<br>5.5           | 3.86<br>4.86      | 3.76<br>4.76  |      |
| V <sub>OL</sub>    | Maximum Low-Level Output Voltage               | I <sub>OUT</sub> ≤ 50 μA   | 4.5<br>5.5           | 0.1<br>0.1        | 0.1<br>0.1    | V    |
|                    |  | *V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OL</sub> = 24 mA<br>I <sub>OL</sub> = 24 mA  | 4.5<br>5.5           | 0.36<br>0.36      | 0.44<br>0.44  |      |
| I <sub>IN</sub>    | Maximum Input Leakage Current                  | V <sub>IN</sub> = V <sub>CC</sub> or GND   | 5.5                  | ±0.1              | ±1.0          | μA   |
| ΔI <sub>CC</sub> T | Additional Max. I <sub>CC</sub> /Input         | V <sub>IN</sub> = V <sub>CC</sub> - 2.1 V  | 5.5                  |                   | 1.5           | mA   |
| I <sub>OZ</sub>    | Maximum Three-State Leakage Current            | V <sub>IN</sub> (OE) = V <sub>IH</sub> or V <sub>IL</sub><br>V <sub>IN</sub> = V <sub>CC</sub> or GND<br>V <sub>OUT</sub> = V <sub>CC</sub> or GND | 5.5                  | ±0.6              | ±6.0          | μA   |
| I <sub>OLD</sub>   | +Minimum Dynamic Output Current                | V <sub>OLD</sub> = 1.65 V Max  | 5.5                  |                   | 75            | mA   |
| I <sub>OHD</sub>   | +Minimum Dynamic Output Current                | V <sub>OHD</sub> = 3.85 V Min  | 5.5                  |                   | -75           | mA   |
| I <sub>CC</sub>    | Maximum Quiescent Supply Current (per Package) | V <sub>IN</sub> = V <sub>CC</sub> or GND   | 5.5                  | 8.0               | 80            | μA   |

\* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

**AC ELECTRICAL CHARACTERISTICS**( $V_{CC}=5.0\text{ V} \pm 10\%$ ,  $C_L=50\text{pF}$ , Input  $t_r=t_f=3.0\text{ ns}$ )

| Symbol    | Parameter  | Guaranteed Limits |      |               |      | Unit |
|-----------|--|-------------------|------|---------------|------|------|
|           |  | 25 °C             |      | -40°C to 85°C |      |      |
|           |  | Min               | Max  | Min           | Max  |      |
| $t_{PLH}$ | Propagation Delay, A to B, B to A (Figure 1)                       | 1.5               | 7.5  | 1.5           | 8.0  | ns   |
| $t_{PHL}$ | Propagation Delay, A to B, B to A (Figure 1)                       | 1.5               | 8.0  | 1.0           | 9.0  | ns   |
| $t_{PZH}$ | Propagation Delay, Direction or Output Enable to A or B (Figure 2) | 1.5               | 10.0 | 1.5           | 11.0 | ns   |
| $t_{PZL}$ | Propagation Delay, Direction or Output Enable to A or B (Figure 2) | 1.5               | 10.0 | 1.5           | 12.0 | ns   |
| $t_{PHZ}$ | Propagation Delay, Direction or Output Enable to A or B (Figure 2) | 1.5               | 10.0 | 1.0           | 11.0 | ns   |
| $t_{PLZ}$ | Propagation Delay, Direction or Output Enable to A or B (Figure 2) | 2.0               | 10.0 | 1.5           | 11.0 | ns   |
| $C_{IN}$  | Maximum Input Capacitance  | 4.5               |      | 4.5           |      | pF   |
| $C_{OUT}$ | Maximum Three-State I/O Capacitance (I/O in High-Impedance State)  | 15                |      | 15            |      | pF   |

| $C_{PD}$ | Power Dissipation Capacitance | Typical @25°C, $V_{CC}=5.0\text{ V}$ |  | pF |
|----------|-------------------------------|--------------------------------------|--|----|
|          |                               | 45                                   |  |    |
|          |                               |                                      |  |    |

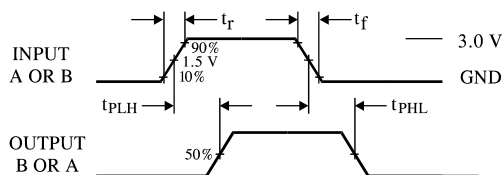


Figure 1. Switching Waveforms

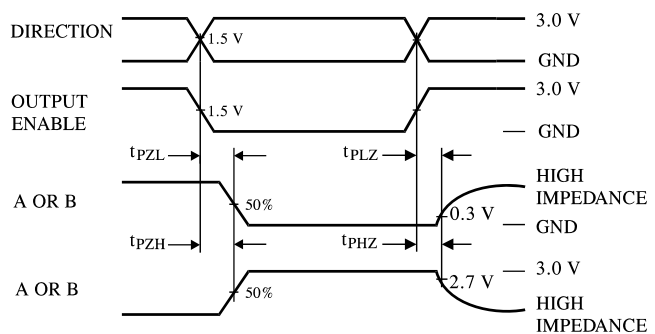


Figure 2. Switching Waveforms

EXPANDED LOGIC DIAGRAM

