

**IN74LV74**

**Dual D-type flip-flop with set and reset;  
positive-edge trigger**

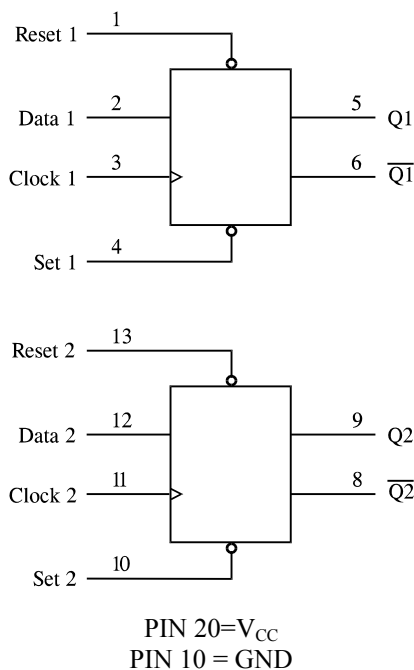
The IN74LV74 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT74.

The IN74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set (S<sub>D</sub>) and (R<sub>D</sub>) inputs; also complementary  $\bar{Q}$  and Q outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC<sub>S</sub>
- Supply voltage range: 1.2 to 3.6 V
- Low input current: 1.0  $\mu$ A; 0.1  $\mu$ A at T = 25 °C
- High Noise Immunity Characteristic of CMOS Devices

**LOGIC DIAGRAM**



N SUFFIX PLASTIC

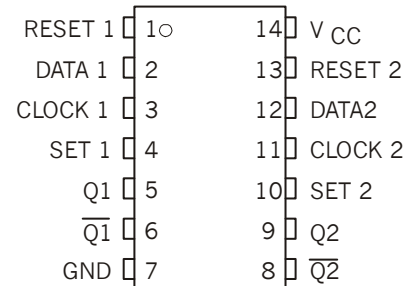
D SUFFIX SOIC

**ORDERING INFORMATION**

**IN74LV74N** Plastic DIP  
**IN74LV74D** SOIC  
**IZ74LV74** chip

T<sub>A</sub> = -40° to 125° C for all packages

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H		H	H	L
H	H		L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H		X	No Change	

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

H= high level  
X = don't care

L = low level  
Z = high impedance

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC supply voltage	-0.5 to +5.0	V
I <sub>IK</sub> * <sup>1</sup>	Input diode current	±20	mA
I <sub>OK</sub> * <sup>2</sup>	Output diode current	±50	mA
I <sub>O</sub> * <sup>3</sup>	Output source or sink current	±35	mA
I <sub>CC</sub>	V <sub>CC</sub> current	±70	mA
I <sub>GND</sub>	GND current	±70	mA
P <sub>D</sub>	Power dissipation per package: Plastic DIP * <sup>4</sup> SO * <sup>4</sup>	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

\*<sup>1</sup> V<sub>I</sub> < -0.5 V or V<sub>I</sub> > V<sub>CC</sub> + 0.5 V.

\*<sup>2</sup> V<sub>O</sub> < -0.5 V or V<sub>O</sub> > V<sub>CC</sub> + 0.5 V.

\*<sup>3</sup> -0.5 V < V<sub>O</sub> < V<sub>CC</sub> + 0.5 V.

\*<sup>4</sup> Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C  
SO Package: - 8 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	1.2	3.6	V
V <sub>I</sub>	DC Input Voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time except for Schmitt-trigger inputs (Figure 1)	V <sub>CC</sub> = 1.2 V V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 3.0 V V <sub>CC</sub> = 3.6 V	0 1000 700 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit						Unit	
				25°C		-40°C to 85°C		125°C			
				min	max	min	max	min	max		
V <sub>IH</sub>	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	V	
			2.0	1.4	-	1.4	-	1.4	-		
			3.0	2.1	-	2.1	-	2.1	-		
			3.6	2.5	-	2.5	-	2.5	-		
V <sub>IL</sub>	LOW level output voltage		1.2	-	0.3	-	0.3	-	0.3	V	
			2.0	-	0.6	-	0.6	-	0.6		
			3.0	-	0.9	-	0.9	-	0.9		
			3.6	-	1.1	-	1.1	-	1.1		
V <sub>OH</sub>	HIGH level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V	
			2.0	1.92	-	1.9	-	1.9	-		
			3.0	2.92	-	2.9	-	2.9	-		
			3.6	3.52	-	3.5	-	3.5	-		
			V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -6mA	3.0	2.48	-	2.34	-	2.20	-	V
		V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 μA	1.2	-	0.09	-	0.1	-	0.1
2.0	-				0.09	-	0.1	-	0.1		
3.0	-				0.09	-	0.1	-	0.1		
3.6	-				0.09	-	0.1	-	0.1		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 6 mA			3.0	-	0.33	-	0.4	-	0.5	V
I <sub>I</sub>	Input current			V <sub>I</sub> = V <sub>CC</sub> or 0 V	*	-	±0.1	-	±1.0	-	±1.0
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0 V I <sub>O</sub> = 0 μA	*	-	4.0	-	40	-	80	μA	

\* V<sub>CC</sub> = 3.3 ± 0.3 V

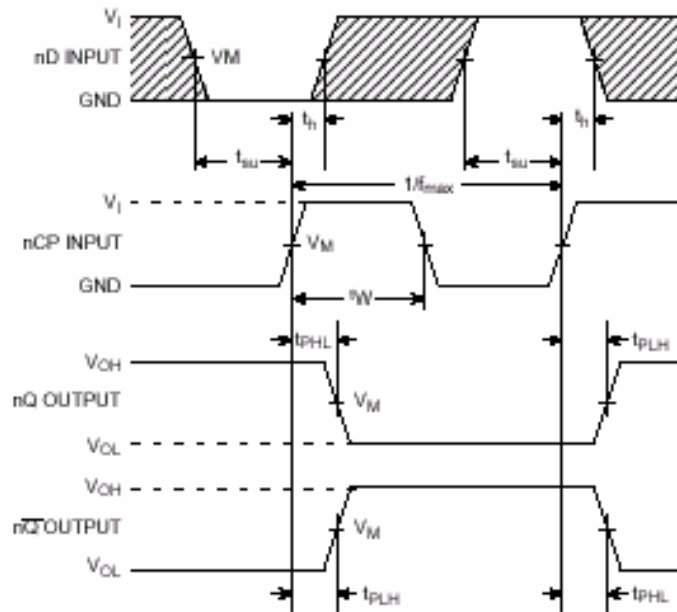
**AC ELECTRICAL CHARACTERISTICS** (C<sub>I</sub>=50 pF, t<sub>r</sub>=t<sub>f</sub>=6.0 ns)

Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay, Clock to Q or Q	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 1,3	1.2	-	140	-	160	-	180	ns
			2.0	-	45	-	56	-	67	
			*	-	28	-	35	-	42	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay, Set to Q or Q	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 2,3	1.2	-	150	-	170	-	190	ns
			2.0	-	44	-	54	-	65	
			*	-	27	-	34	-	41	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay, Reset to Q or Q	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 2,3	1.2	-	160	-	180	-	200	ns
			2.0	-	47	-	58	-	70	
			*	-	29	-	37	-	44	
t <sub>THL</sub> , t <sub>TLH</sub>	Output Transition Time, Any Output	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 1,3	1.2	-	90	-	110	-	130	ns
			2.0	-	20	-	25	-	30	
			*	-	15	-	19	-	23	
C <sub>I</sub>	Input capacitance		3.0	-	7.0	-	-	-	-	pF
C <sub>PD</sub>	Power dissipation capacitance (per flip-flop)	V <sub>I</sub> = 0 V or V <sub>CC</sub>		-	48	-	-	-	-	pF

**TIMING REQUIREMENTS**( $C_L=50$  pF,  $t_r=t_f=6.0$  ns)

Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t <sub>w</sub>	Pulse Width, Clock, Set or Reset	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 1,2,3	1.2	75	-	96	-	114	-	ns
			2.0	25	-	32	-	38	-	
			*	16	-	20	-	24	-	
t <sub>su</sub>	Setup Time, Data to Clock	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 1,3	1.2	25	-	32	-	40	-	ns
			2.0	16	-	20	-	24	-	
			*	10	-	13	-	15	-	
t <sub>rem</sub>	Removal Time, Set or Reset to Clock	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 2,3	1.2	18	-	24	-	30	-	ns
			2.0	9	-	12	-	15	-	
			*	6	-	8	-	9	-	
t <sub>h</sub>	Hold Time, Clock to Data	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 1,3	1.2	3	-	5	-	5	-	ns
			2.0	3	-	3	-	3	-	
			*	3	-	3	-	3	-	
f <sub>c</sub>	Clock Frequency	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figures 1,3	1.2	8	-	6	-	4	-	MHz
			2.0	18	-	15	-	12	-	
			3.0	30	-	24	-	20	-	

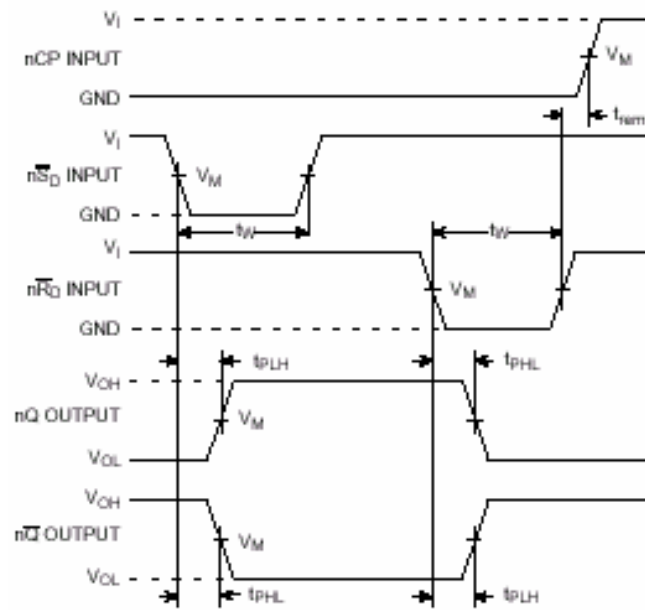
\* V<sub>CC</sub> = 3.3 ± 0.3 V



$V_M = 0.5 * V_{CC}$

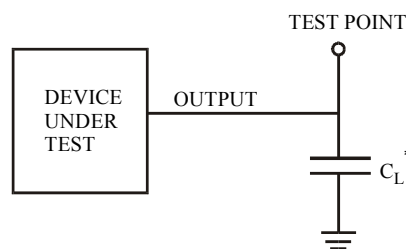
V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.

Figure 1. Switching Waveforms



$$V_M = 0.5 * V_{CC}$$

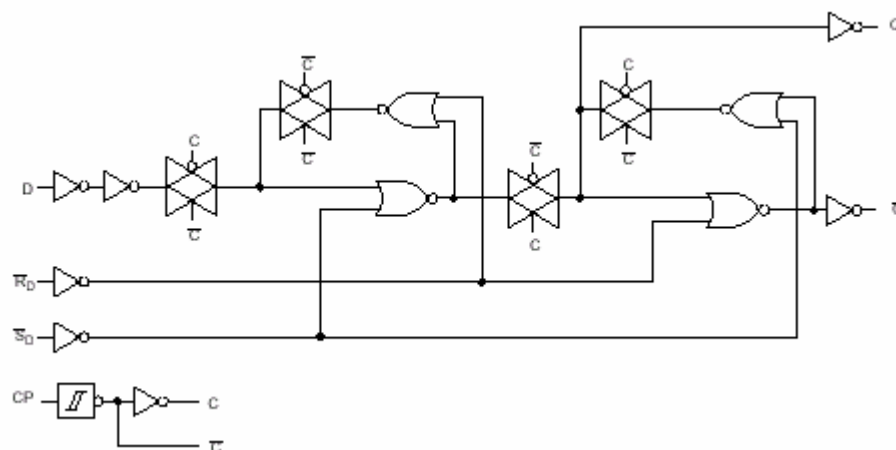
Figure 2. Switching Waveforms



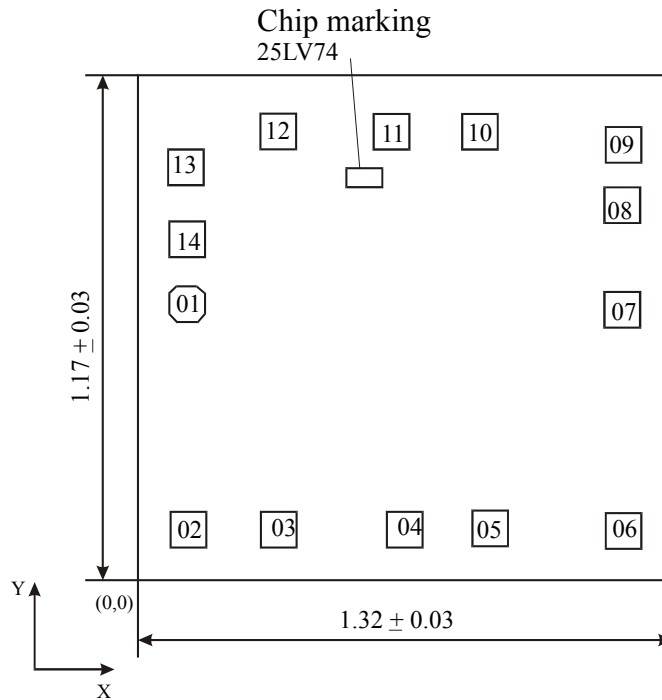
\* Includes all probe and jig capacitance

Figure 3. Test Circuit

**EXPANDED LOGIC DIAGRAM  
(ONE FLIP-FLOP)**



## CHIP PAD DIAGRAM



**Location of marking (mm):** left lower corner  $x=0.520$ ,  $y=0.865$ .

**Chip thickness:**  $0.46 \pm 0.02$  mm.

## PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Reset 1	0.118	0.436	0.108 x 0.108
02	Data 1	0.118	0.125	0.108 x 0.108
03	Clock 1	0.286	0.125	0.108 x 0.108
04	Set 1	0.597	0.125	0.108 x 0.108
05	$\overline{Q} 1$	0.895	0.125	0.108 x 0.108
06	$\overline{Q} 1$	1.100	0.125	0.108 x 0.108
07	GND	1.100	0.423	0.108 x 0.108
08	$\overline{Q} 2$	1.100	0.721	0.108 x 0.108
09	Q 2	1.100	0.930	0.108 x 0.108
10	Set 2	0.851	0.949	0.108 x 0.108
11	Clock 2	0.540	0.949	0.108 x 0.108
12	Data 2	0.297	0.949	0.108 x 0.108
13	Reset 2	0.118	0.830	0.108 x 0.108
14	$V_{CC}$	0.118	0.604	0.108 x 0.108

Note: Pad location is given as per metallization layer