

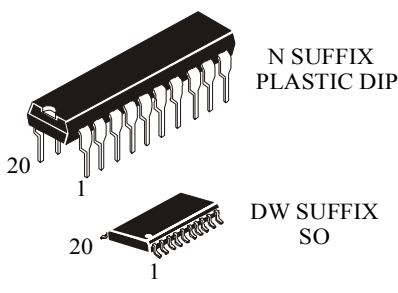
IN74LV574

**Octal D-type flip-flop;
positive edge-trigger (3-State)**

The 74LV574 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT574.

The 74LV574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for oriented applications. A clock (CP) and an output enable (OE) input are common to all flip-flops. The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When OE is LOW, the contents of the eight flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the flip-flops.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL ICs
- Supply voltage range: 1.0 to 5.5 V
- Low input current: 1.0 μ A; 0.1 μ A at T = 25 °C
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC DIP

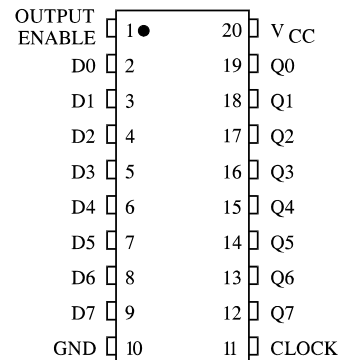
DW SUFFIX
SO

ORDERING INFORMATION

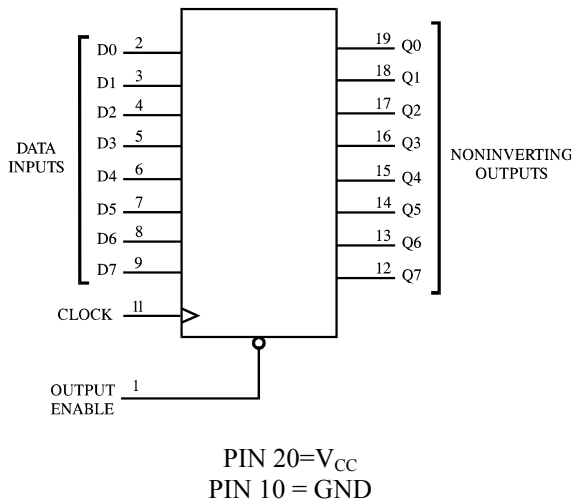
IN74LV574N Plastic DIP
IN74LV574DW SOIC
IZ74LV574 chip

T_A = -40° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Output Enable	Inputs		Output
	Clock	D	Q
L		H	H
L		L	L
L	L,H,	X	no change
H	X	X	Z

H= high level
L = low level
X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC supply voltage	-0.5 to +7.0	V
I _{IK} * ¹	Input diode current	±20	mA
I _{OK} * ²	Output diode current	±50	mA
I _O * ³	Output source or sink current	±35	mA
I _{CC}	V _{CC} current	±70	mA
I _{GND}	GND current	±70	mA
P _D	Power dissipation per package: Plastic DIP * ⁴ SO * ⁴	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

*¹ V_I < -0.5 V or V_I > V_{CC} + 0.5 V.

*² V_O < -0.5 V or V_O > V_{CC} + 0.5 V.

*³ -0.5 V < V_O < V_{CC} + 0.5 V.

*⁴ Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C

SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	1.0	5.5	V
V _I	DC Input Voltage	0	V _{CC}	V
V _O	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			ns
	0 V ≤ V _{CC} ≤ 2.0 V	0	500	
	2.0 V ≤ V _{CC} ≤ 2.7 V	0	200	
	2.7 V ≤ V _{CC} ≤ 3.6 V	0	100	
	3.6 V ≤ V _{CC} ≤ 5.5 V	0	50	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

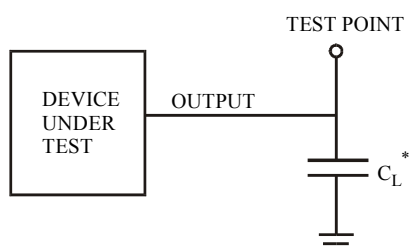
DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V _{CC} V	Guaranteed Limit								Unit
				25°C		-40°C		85°C		125°C		
				min	max	min	max	min	max	min	max	
V _{IH}	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	1.4	-	
			2.7	2.0	-	2.0	-	2.0	-	2.0	-	
			3.0	2.0	-	2.0	-	2.0	-	2.0	-	
			3.6	2.0	-	2.0	-	2.0	-	2.0	-	
			4.5	3.15	-	3.15	-	3.15	-	3.15	-	
			5.5	3.85	-	3.85	-	3.85	-	3.85	-	
V _{IL}	LOW level output voltage		1.2	-	0.3	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	-	0.6	
			2.7	-	0.8	-	0.8	-	0.8	-	0.8	
			3.0	-	0.8	-	0.8	-	0.8	-	0.8	
			3.6	-	0.8	-	0.8	-	0.8	-	0.8	
			4.5	-	1.35	-	1.35	-	1.35	-	1.35	
			5.5	-	1.65	-	1.65	-	1.65	-	1.65	
V _{OH}	HIGH level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	1.2	1.05	-	1.05	-	1.0	-	1.0	-	V
			2.0	1.85	-	1.85	-	1.8	-	1.8	-	
			2.7	2.55	-	2.55	-	2.5	-	2.5	-	
			3.0	2.85	-	2.85	-	2.8	-	2.8	-	
			3.6	3.45	-	3.45	-	3.4	-	3.4	-	
			4.5	4.35	-	4.35	-	4.3	-	4.3	-	
V _{OL}	LOW level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	1.2	-	0.15	-	0.15	-	0.2	-	0.2	V
			2.0	-	0.15	-	0.15	-	0.2	-	0.2	
			2.7	-	0.15	-	0.15	-	0.2	-	0.2	
V _{OL}	LOW level output voltage	V _I = V _{IH} or V _{IL} I _O = 8 mA	3.0	-	0.15	-	0.15	-	0.2	-	0.2	V
			3.6	-	0.15	-	0.15	-	0.2	-	0.2	
			4.5	-	0.15	-	0.15	-	0.2	-	0.2	
V _{OL}	LOW level output voltage	V _I = V _{IH} or V _{IL} I _O = 16 mA	5.5	-	0.15	-	0.15	-	0.2	-	0.2	V
			3.0	-	0.33	-	0.33	-	0.40	-	0.50	
			4.5	-	0.40	-	0.40	-	0.55	-	0.65	
I _I	Input current	V _I = V _{CC} or 0 V	5.5	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	Supply current	V _I = V _{CC} or 0 V I _O = 0 μA	5.5	-	8.0	-	8.0	-	20	-	160	μA
I _{CC1}	Additional supply current per input	V _I = V _{CC} - 0.6V	2.7 3.6	-	0.2	-	0.2	-	0.5	-	0.85	mA
I _{OZ}	Three state leakage current	3-state output V _I (11) = V _{IH} V _O = V _{CC} or 0 V	5.5	-	±0.5	-	±0.5	-	±5	-	±10	μA

AC ELECTRICAL CHARACTERISTICS ($C_L=50$ pF, $t_r=t_f=2.5$ ns)

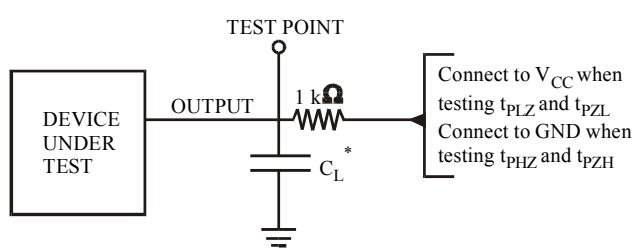
Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_{PHL} , t_{PLH}	Propagation delay, Clock to Q	$V_1 = 0$ V or V_1 Figures 1,3	1.2	-	160	-	170	-	200	ns
			2.0	-	26	-	34	-	43	
			2.7	-	20	-	25	-	31	
			3.0	-	16	-	20	-	25	
			4.5	-	14	-	17	-	21	
t_{PHZ} , t_{PLZ}	Propagation delay, OE to Q	$V_1 = 0$ V or V_1 Figures 2,4	1.2	-	160	-	170	-	200	ns
			2.0	-	31	-	39	-	48	
			2.7	-	23	-	29	-	36	
			3.0	-	20	-	24	-	29	
			4.5	-	17	-	20	-	24	
t_{PZH} , t_{PZL}	Propagation delay, OE to Q	$V_1 = 0$ V or V_1 Figures 2,4	1.2	-	140	-	160	-	180	ns
			2.0	-	26	-	34	-	43	
			2.7	-	20	-	25	-	31	
			3.0	-	16	-	20	-	25	
			4.5	-	14	-	17	-	21	
C_I	Input capacitance		5.5	-	7.0*	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per flip-flop)	$V_1 = 0$ V or V_{CC}	5.5	-	50*	-	-	-	-	pF

* T = 25°C



* Includes all probe and jig capacitance

Figure 1. Test Circuit

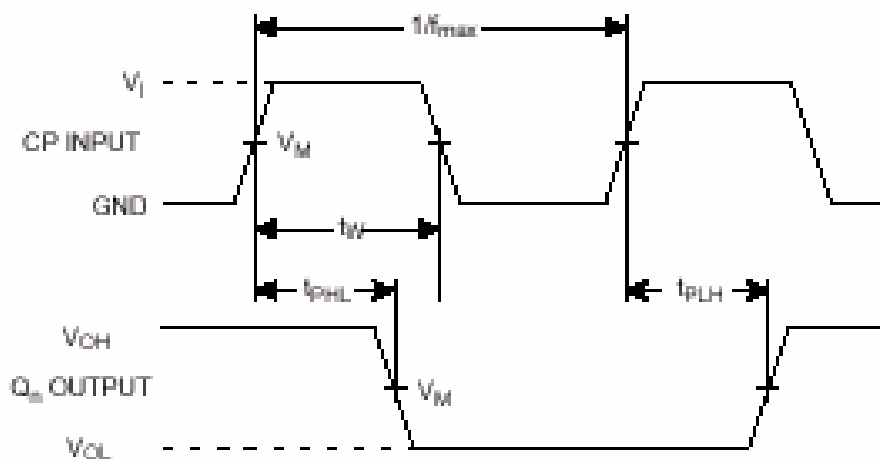


* Includes all probe and jig capacitance

Figure 2. Test Circuit

TIMING REQUIREMENTS($C_L=50$ pF, $t_r=t_f=2.5$ ns)

Symbol	Parameter	Test conditions	V _{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t _w	Pulse Width, Clock (high)	V _I = 0 V or V _I Figures 1,3	1.2	120	-	-	-	-	-	ns
			2.0	29	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	17	-	20	-	24	-	
			4.5	15	-	-	-	-	-	
t _{su}	Setup Time, Data to Clock	V _I = 0 V or V _I Figures 1,5	1.2	40	-	-	-	-	ns	
			2.0	19	-	22	-	26		-
			2.7	14	-	16	-	19		-
			3.0	11	-	13	-	15		-
			4.5	9	-	-	-	-		-
t _h	Hold Time, Clock to Data	V _I = 0 V or V _I Figures 1,5	1.2	5	-	5	-	5	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
f _c	Clock Frequency	V _I = 0 V or V _I Figures 1,3	1.2	-	2	-	-	-	MHz	
			2.0	-	17	-	15	-		12
			2.7	-	21	-	19	-		16
			3.0	-	27	-	24	-		20
			4.5	-	31	-	-	-		-



V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Figure 3. Switching Waveforms

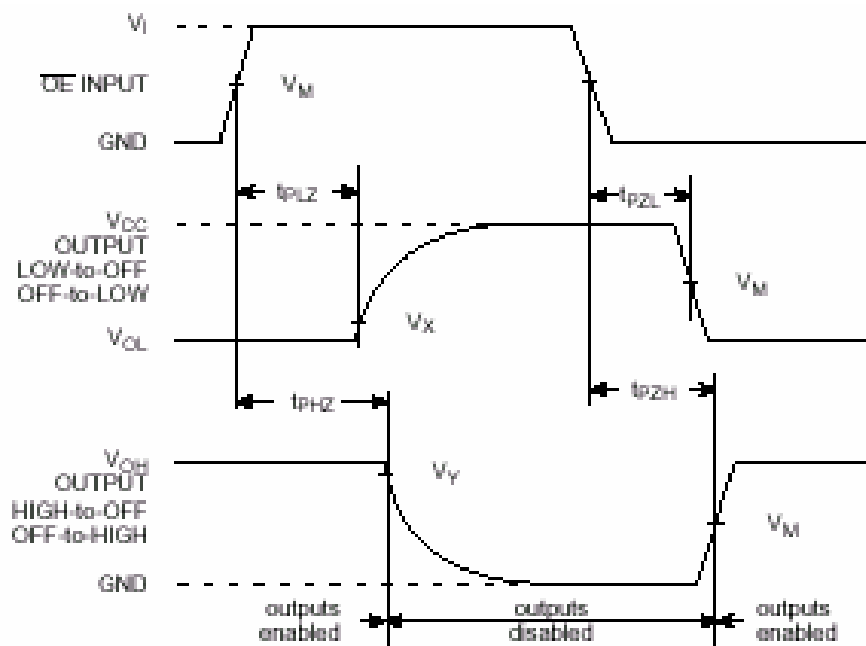


Figure 4. Switching Waveforms

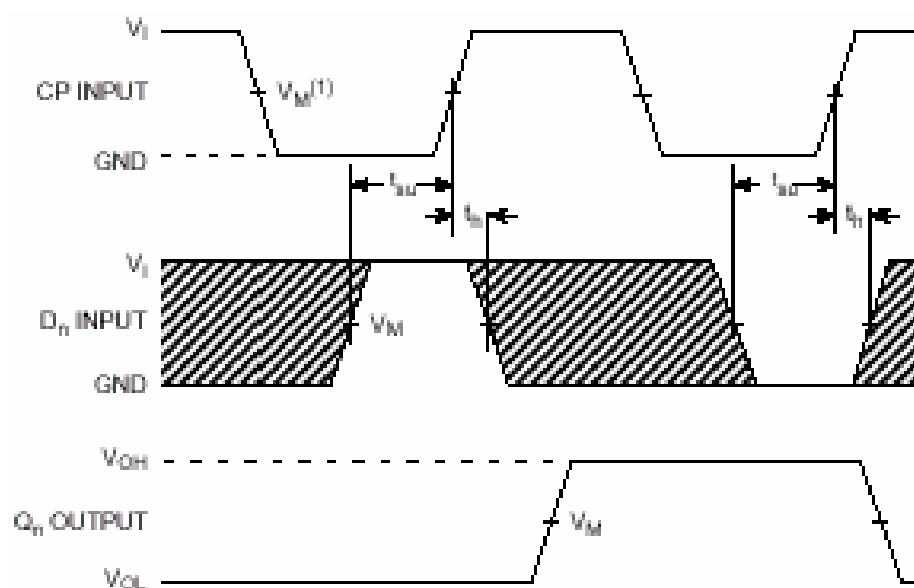
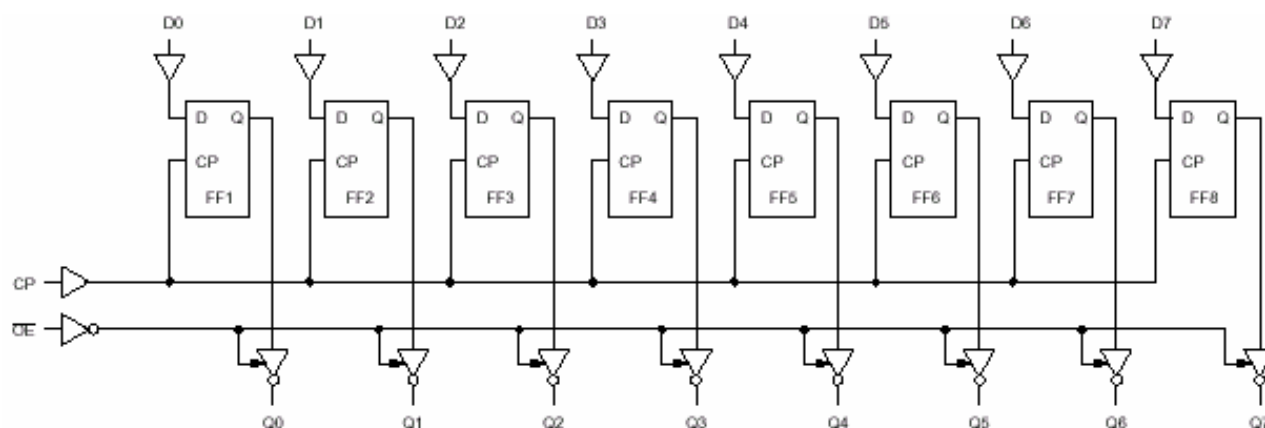


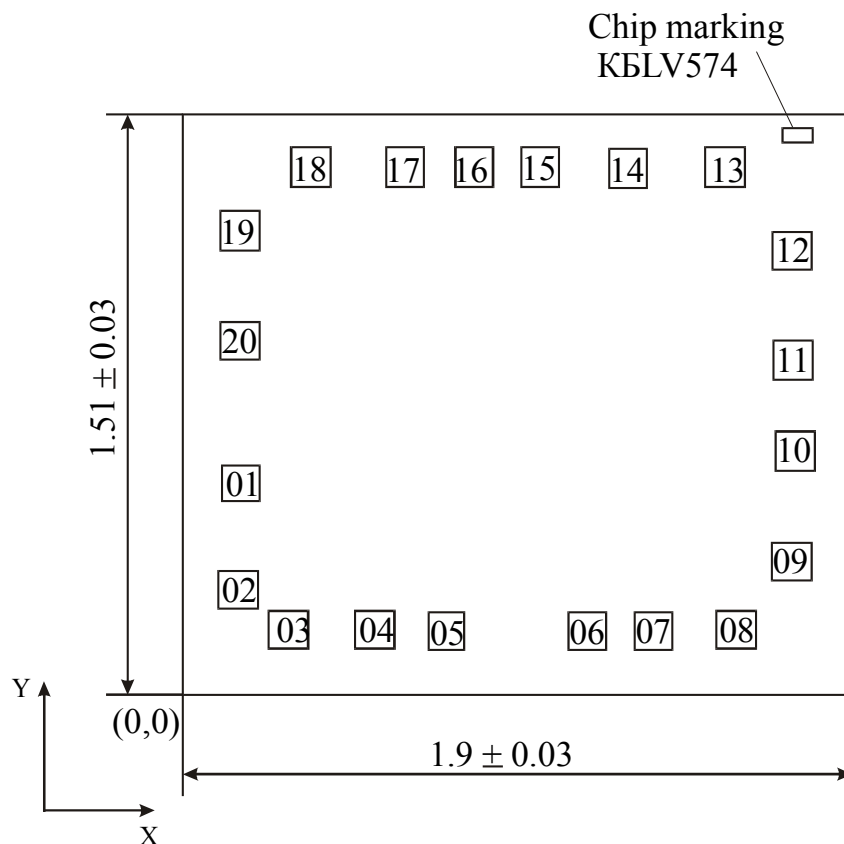
Figure 5. Switching Waveforms

Symbol	V _{CC} , V	Temperature, °C					
		-40°C to 25		85		125	
		Level of a signal					
		V	%	V	%	V	%
V _I	1.2	1.2	-	1.2	-	1.2	-
	2.0	2.0	-	2.0	-	2.0	-
	2.7	2.7	-	2.7	-	2.7	-
	3.0	3.0	-	3.0	-	3.0	-
	4.5	4.5	-	4.5	-	4.5	-
V _M INPUTS	1.2	0.6	50	0.6	50	0.6	50
	2.0	1.0	50	1.0	50	1.0	50
	2.7	1.5	56	1.5	56	1.5	56
	3.0	1.5	56	1.5	56	1.5	56
	4.5	2.25	50	2.25	50	2.25	50
V _M OUTPUTS	1.2	0.6	50	0.6	50	0.6	50
	2.0	1.0	50	1.0	50	1.0	50
	2.7	1.5	58	1.5	60	1.5	62
	3.0	1.5	52	1.5	53	1.5	55
	4.5	2.25	50	2.25	50	2.25	50
V _X	1.2	0.32	12	0.37	12.5	0.37	12.5
	2.0	0.4	11	0.45	11	0.45	11
	2.7	0.55	12	0.6	12.5	0.65	12.7
	3.0	0.6	11	0.65	11	0.7	11.5
	4.5	0.85	12	0.90	12	1.0	11
V _Y	1.2	0.88	88	0.78	86.5	0.68	85
	2.0	1.5	88	1.4	87.5	1.3	86.5
	2.7	2.1	87.5	2.0	87	1.9	86
	3.0	2.3	88	2.2	88	2.1	87.5
	4.5	3.45	88	3.35	88	3.25	88

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner $x=1.656$, $y=1.353$.

Chip thickness: 0.46 ± 0.02 mm, (0.35 ± 0.02 mm – for SOIC).

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Output enable	0.128	0.545	0.108 x 0.108
02	D 0	0.128	0.229	0.108 x 0.108
03	D 1	0.330	0.120	0.108 x 0.108
04	D 2	0.576	0.120	0.108 x 0.108
05	D 3	0.738	0.120	0.108 x 0.108
06	D 4	1.054	0.120	0.108 x 0.108
07	D 5	1.216	0.120	0.108 x 0.108
08	D 6	1.466	0.120	0.108 x 0.108
09	D 7	1.682	0.314	0.108 x 0.108
10	GND	1.682	0.533	0.108 x 0.108
11	Clock	1.682	0.839	0.108 x 0.108
12	Q 7	1.682	1.108	0.108 x 0.108
13	Q 6	1.422	1.274	0.108 x 0.108
14	Q 5	1.149	1.274	0.108 x 0.108
15	Q 4	0.971	1.274	0.108 x 0.108
16	Q 3	0.811	1.274	0.108 x 0.108
17	Q 2	0.633	1.274	0.108 x 0.108
18	Q 1	0.360	1.274	0.108 x 0.108
19	Q 0	0.128	1.108	0.108 x 0.108
20	V _{CC}	0.128	0.854	0.108 x 0.108

Note: Pad location is given as per metallization layer